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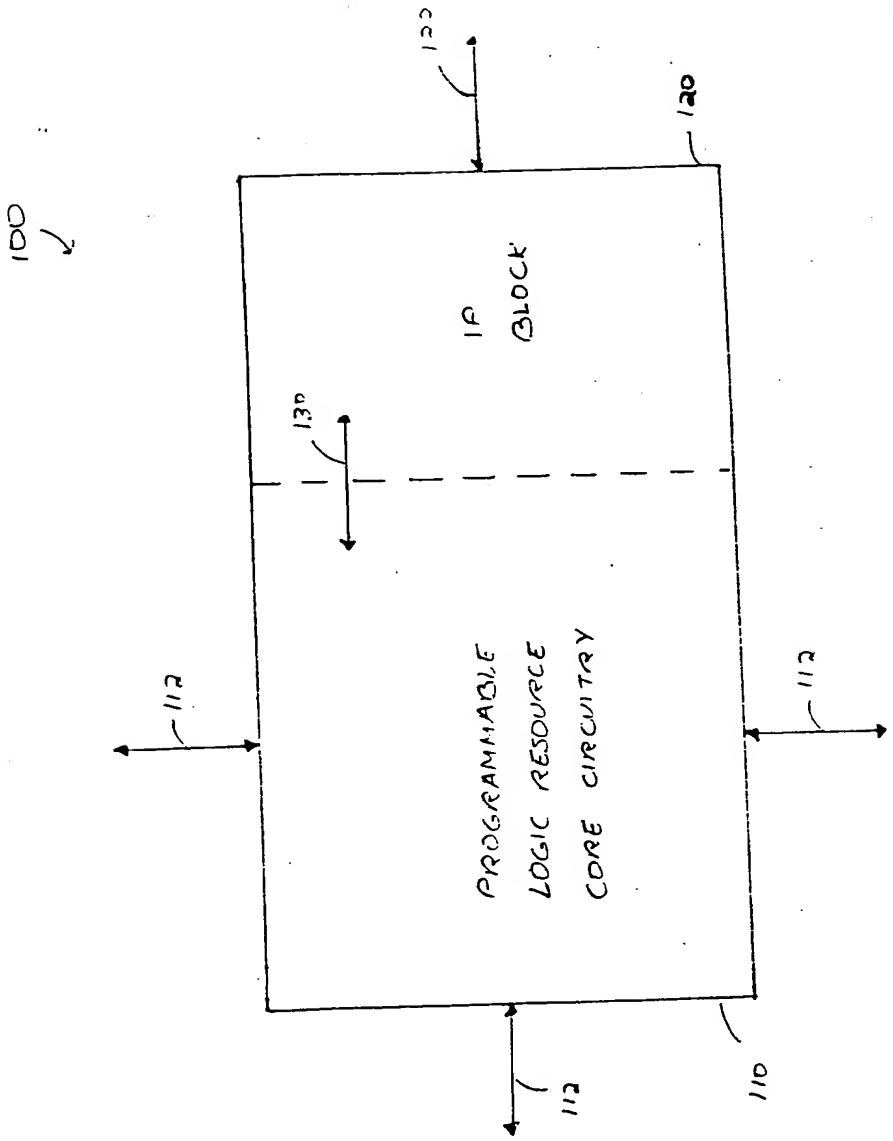
100
122
120
IP BLOCK
130
PROGRAMMABLE LOGIC RESOURCE CORE CIRCUITRY
112
112
112
110

FIG. 1

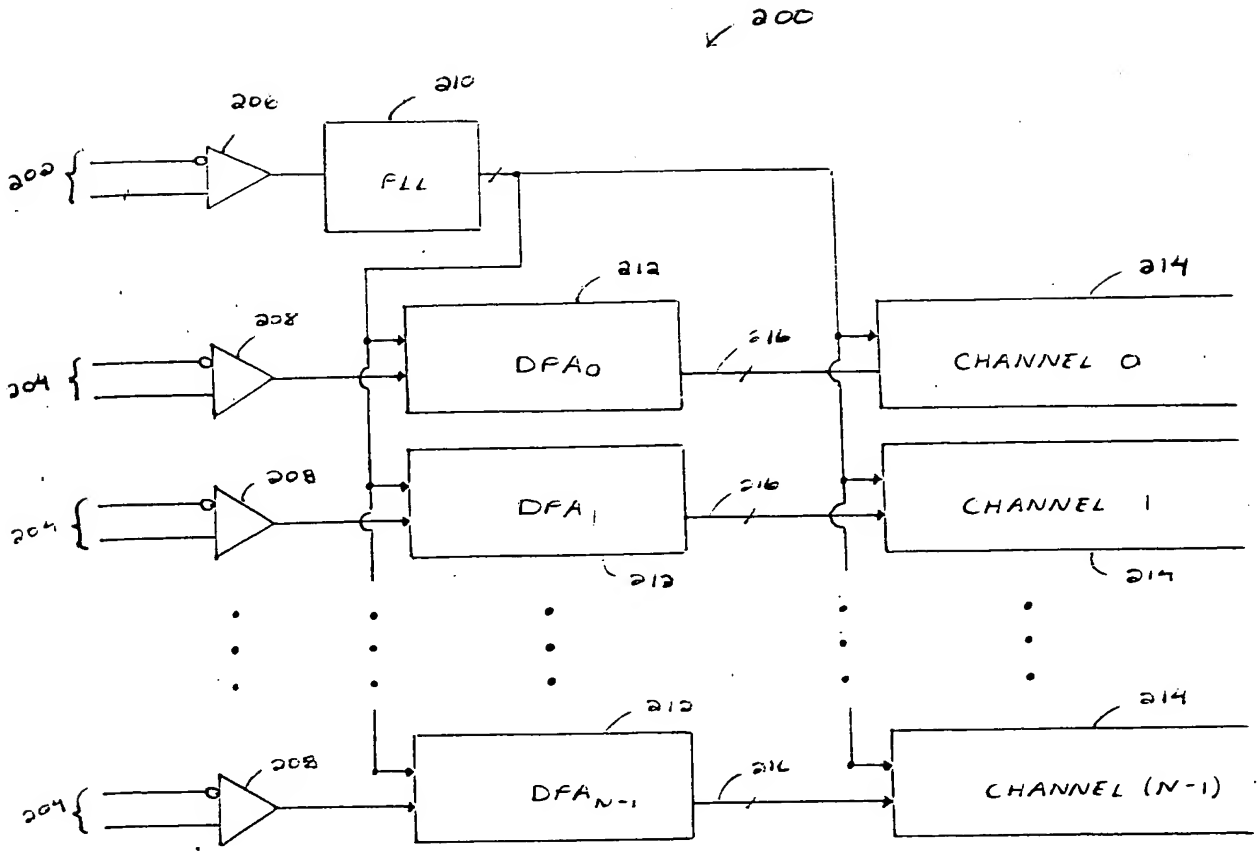
200
202
206
210
FLL
204
208
212
DFA0
216
214
CHANNEL 0
DFA1
CHANNEL 1
DFAN-1
CHANNEL (N-1)

FIG. 2

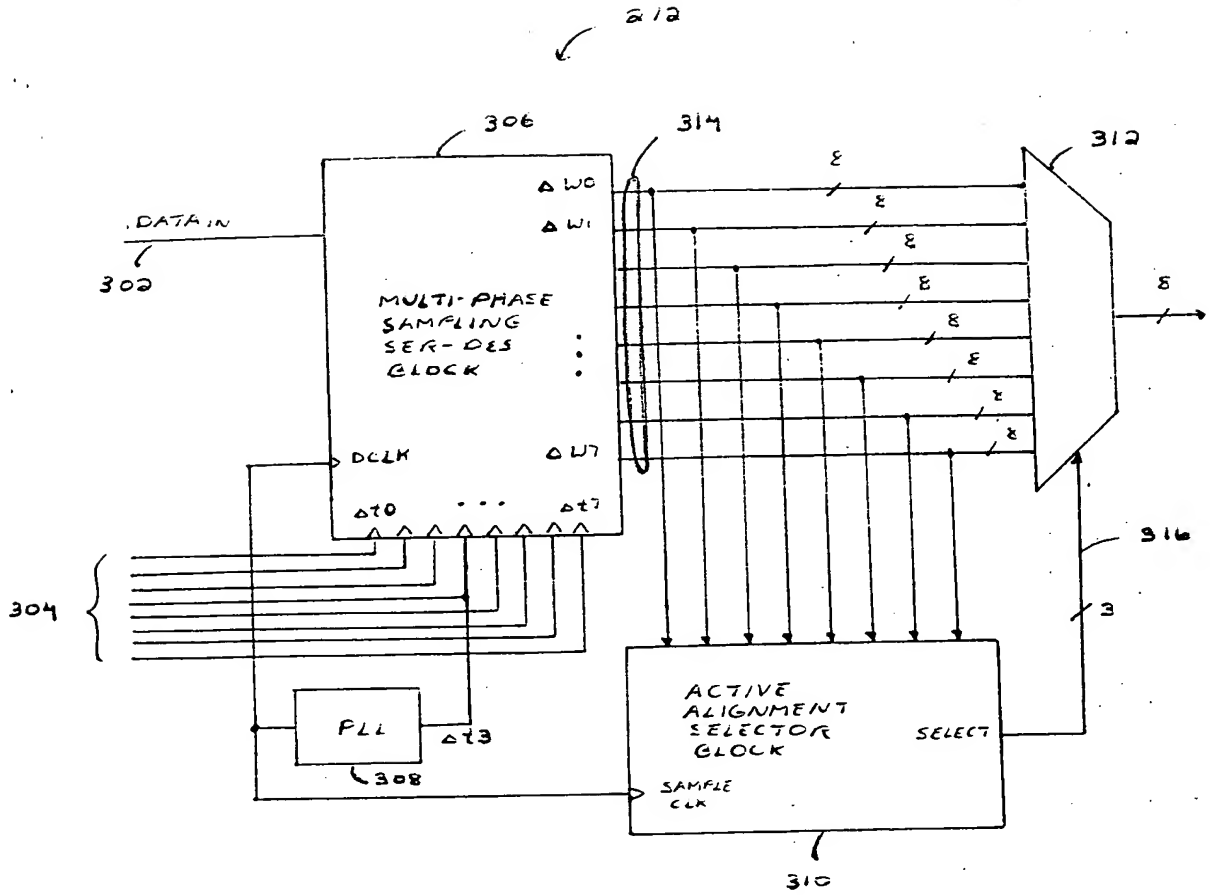
212
306
314
312
DATA IN
302
MULTI-PHASE SAMPLING SER-DES CLOCK
DCLK
304
PLL
308
ACTIVE ALIGNMENT SELECTOR CLOCK
SAMPLE CLK
SELECT
310
316
8
3

FIG. 3

400

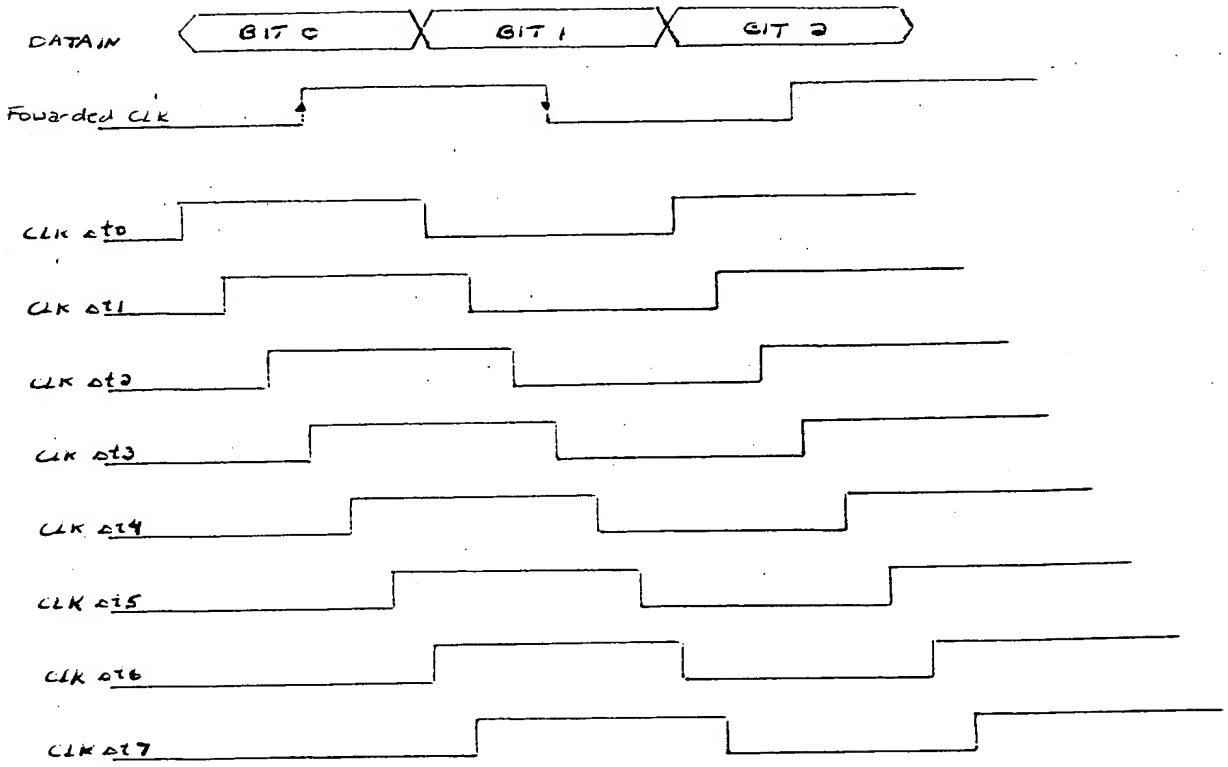
DATAIN
BIT 0
BIT 1
BIT 2
Fowarded CLK
CLK @t0
CLK @t1
CLK @t2
CLK @t3
CLK @t4
CLK @t5
CLK @t6
CLK @t7

FIG 4A

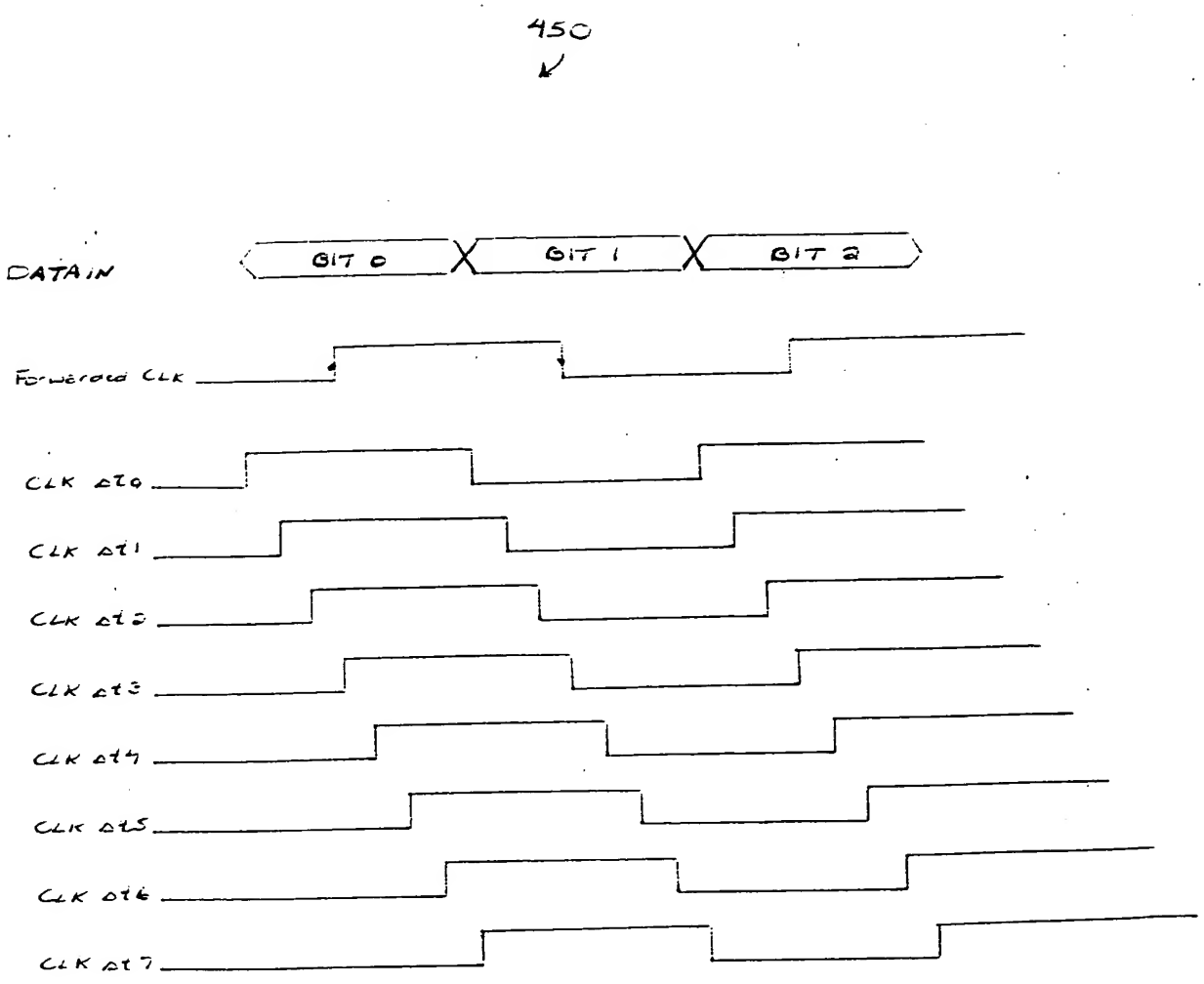
450
DATA IN
BIT 0
BIT 1
BIT 2
Forwarded CLK
CLK Δt0
CLK Δt1
CLK Δt2
CLK Δt3
CLK Δt4
CLK Δt5
CLK Δt6
CLK Δt7

FIG. 4C

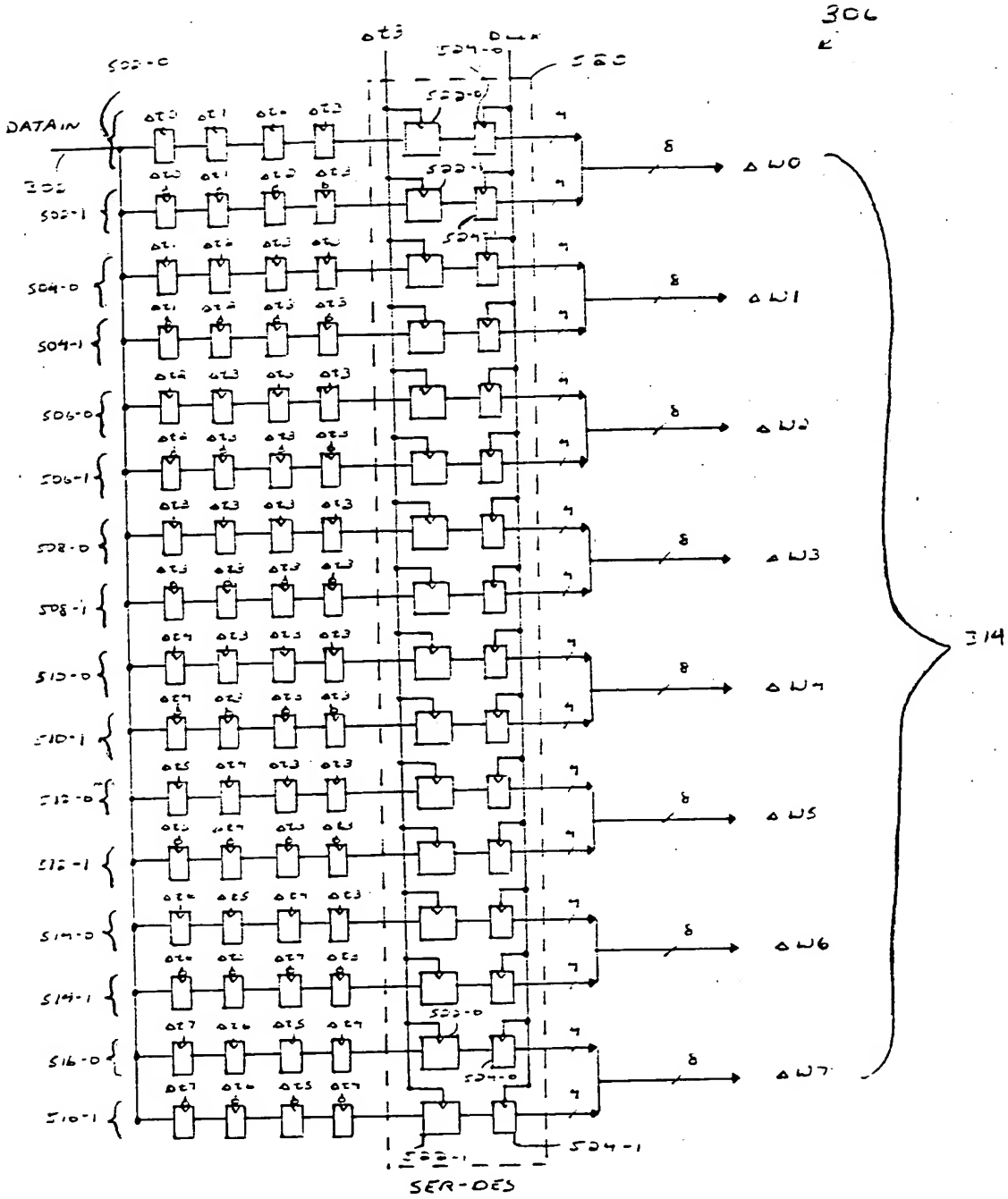

FIG. 5

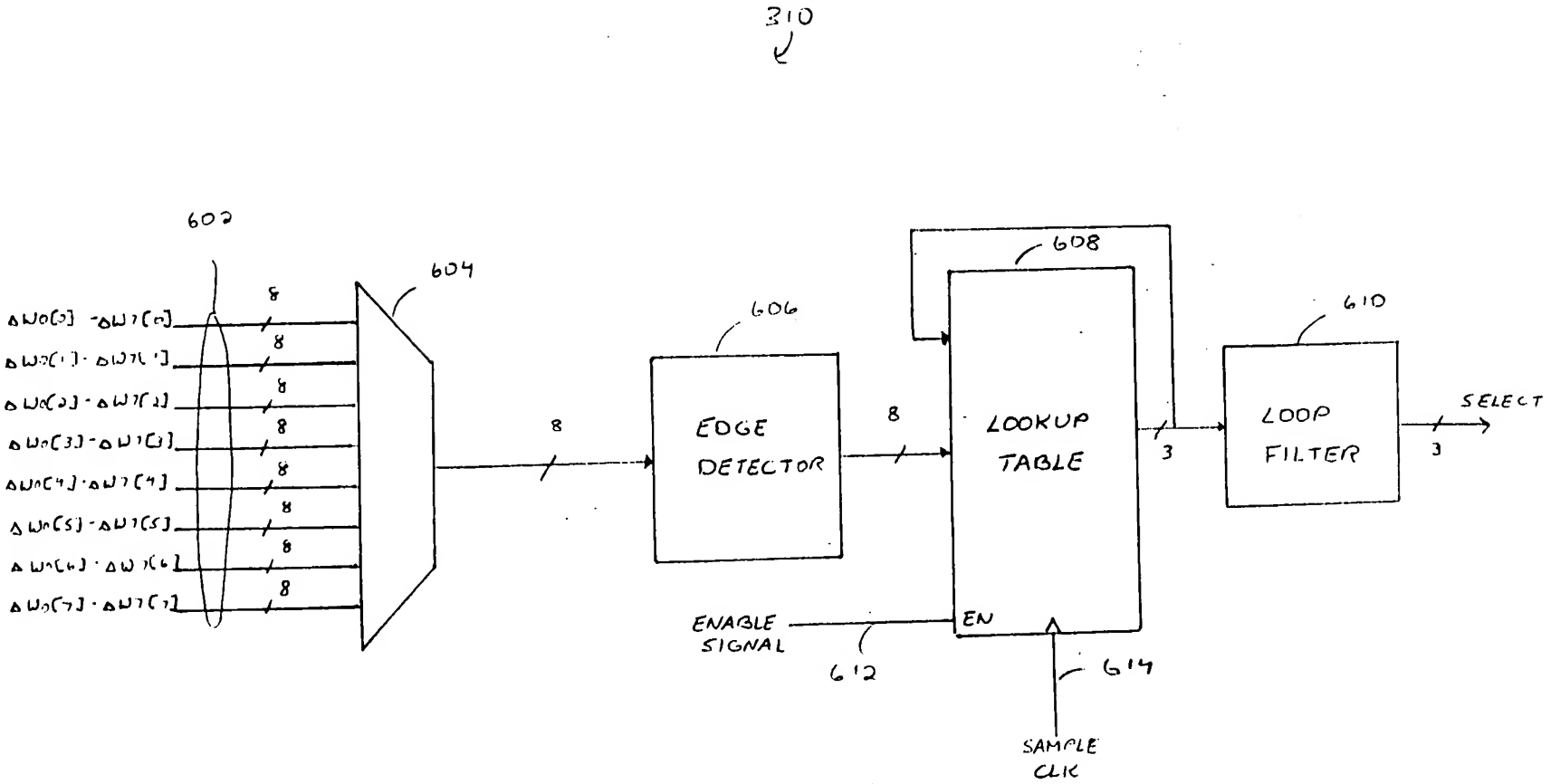
310
602
604
606
608
610
612
614
8
EDGE DETECTOR
LOOKUP TABLE
LOOP FILTER
3
SELECT
ENABLE SIGNAL
EN
SAMPLE CLK

FIG. 6

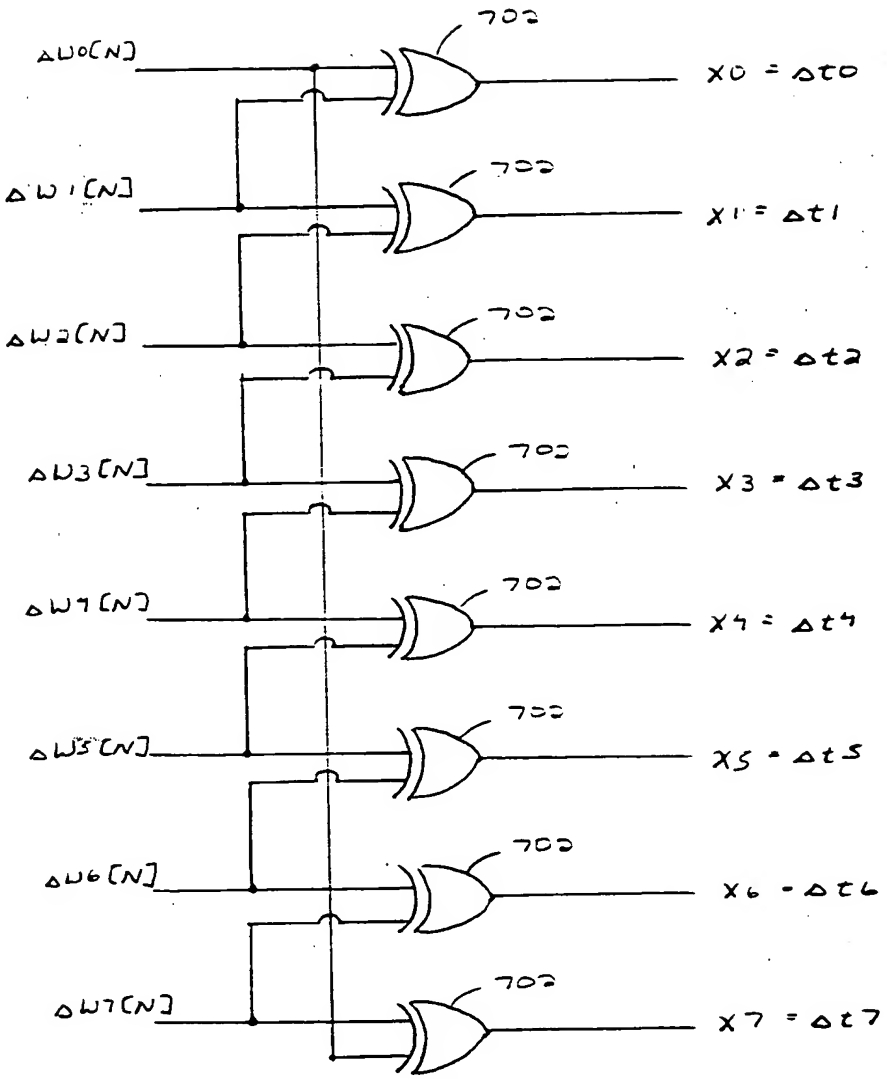
606
702
ΔW0[N]
X0 = Δt0
ΔW1[N]
X1 = Δt1
ΔW2[N]
X2 = Δt2
ΔW3[N]
X3 = Δt3
ΔW4[N]
X4 = Δt4
ΔW5[N]
X5 = Δt5
ΔW6[N]
X6 = Δt6
ΔW7[N]
X7 = Δt7

FIG. 7

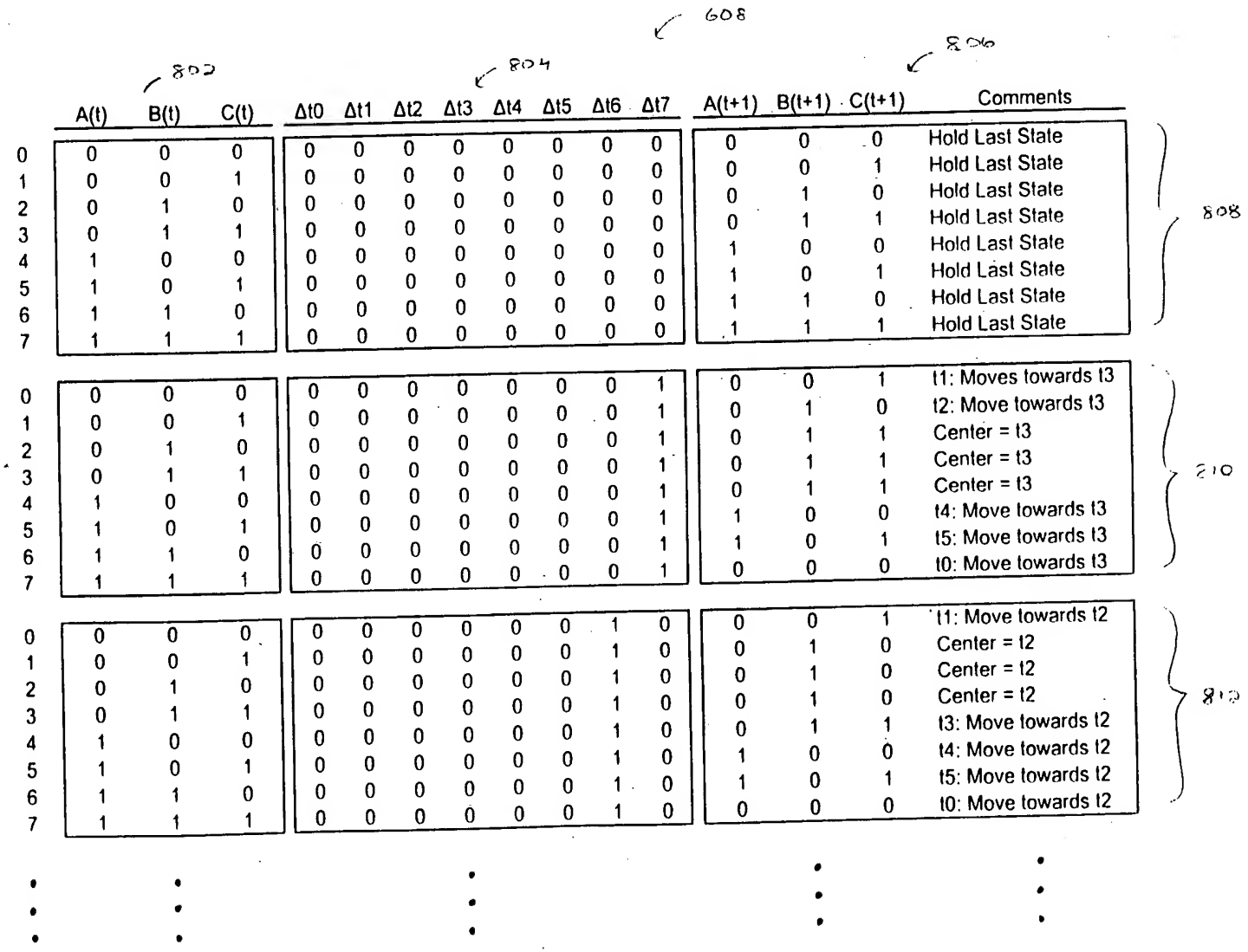
608
802
804
806
A(t) B(t) C(t) Δt0 Δt1 Δt2 Δt3 Δt4 Δt5 Δt6 Δt7 A(t+1) B(t+1) C(t+1) Comments
0 0 0 0 0 0 0 0 0 0 0 0 0 0 Hold Last State
1 0 0 1 0 0 0 0 0 0 0 0 0 1 Hold Last State
2 0 1 0 0 0 0 0 0 0 0 0 1 0 Hold Last State
3 0 1 1 0 0 0 0 0 0 0 0 1 1 Hold Last State
4 1 0 0 0 0 0 0 0 0 0 1 0 0 Hold Last State
5 1 0 1 0 0 0 0 0 0 0 1 0 1 Hold Last State
6 1 1 0 0 0 0 0 0 0 0 1 1 0 Hold Last State
7 1 1 1 0 0 0 0 0 0 0 1 1 1 Hold Last State
808
0 0 0 0 0 0 0 0 0 0 0 0 0 1 t1: Moves towards t3
1 0 0 1 0 0 0 0 0 0 0 0 1 0 t2: Move towards t3
2 0 1 0 0 0 0 0 0 0 0 0 1 1 Center = t3
3 0 1 1 0 0 0 0 0 0 0 0 1 1 Center = t3
4 1 0 0 0 0 0 0 0 0 0 0 1 1 Center = t3
5 1 0 1 0 0 0 0 0 0 0 1 0 0 t4: Move towards t3
6 1 1 0 0 0 0 0 0 0 0 1 0 1 t5: Move towards t3
7 1 1 1 0 0 0 0 0 0 0 0 0 0 t0: Move towards t3
810
0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 t1: Move towards t2
1 0 0 1 0 0 0 0 0 0 1 0 0 1 0 Center = t2
2 0 1 0 0 0 0 0 0 0 1 0 0 1 0 Center = t2
3 0 1 1 0 0 0 0 0 0 1 0 0 1 0 Center = t2
4 1 0 0 0 0 0 0 0 0 1 0 0 1 1 t3: Move towards t2
5 1 0 1 0 0 0 0 0 0 1 0 1 0 0 t4: Move towards t2
6 1 1 0 0 0 0 0 0 0 1 0 1 0 1 t5: Move towards t2
7 1 1 1 0 0 0 0 0 0 1 0 0 0 0 t0: Move towards t2
812

FIG. 8

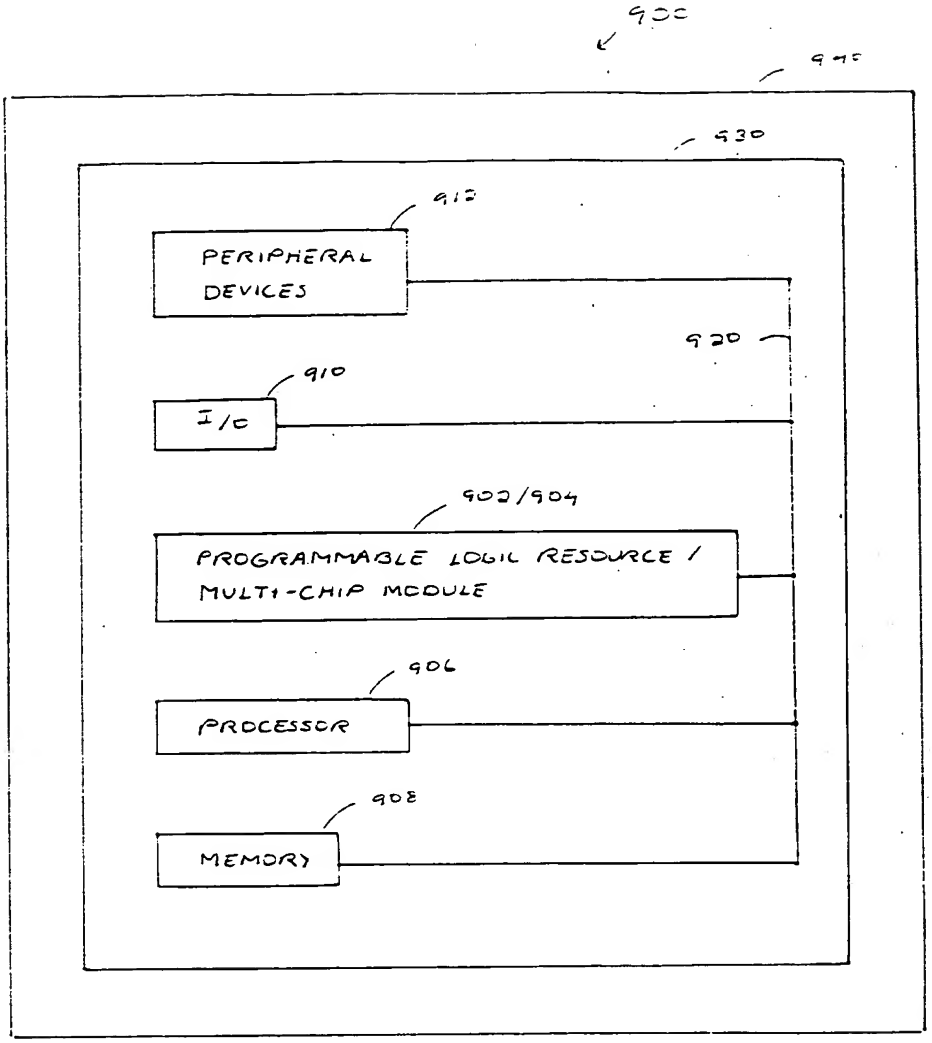
900
940
930
912
PERIPHERAL DEVICES
920
910
I/O
902/904
PROGRAMMABLE LOGIC RESOURCE / MULTI-CHIP MODULE
906
PROCESSOR
908
MEMORY

FIG. 9